REMARKS

Double Patenting

Claims 1-14 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1-46 of U.S. Patent No. 6172549. Applicant does not acquiesce in the Examiner's statements regarding the scope of the claims. Nonetheless, Applicant will submit a terminal disclaimer as an expedient upon the indication of otherwise allowable claims.

Claim Rejections - 35 USC § 112

Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Applicant traverses this rejection.

Claim 14 recites two diode-connected transistors coupled in series between the input terminal and a power supply terminal. The Examiner notes that the two diode-connected transistors shown in Fig. 1 are connected between the base of transistor Q1 and a ground terminal (GND). However, a power supply ground terminal is still considered a power supply terminal. In the case of Fig. 1, it is called ground because it typically provides a zero voltage reference. The circuit of Fig. 1 would also work, however, if the terminal labeled V_{POS} was supplied with zero volts and the terminal labeled GND was supplied with a negative voltage. Both the V_{POS} and GND terminals are power supply terminals, regardless of their actual potential.

Claim Rejections - 35 USC § 102

Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 4,250,457 to Hofmann ("Hofmann"). Applicant traverses this rejection.

Claim 1 is amended to recite limiting the input signal to a range in which the output function of the transistor cell approximates a square-law. Support for this limitation can be found in the specification at page 4, lines 21-21 and elsewhere throughout the specification. Hofmann discloses no such input signal limiting. In fact, Hofmann discloses the desirability of keeping the input signal much larger than the bias current to eliminate nonlinearities. See col. 2, lines 61-64; col. 5, lines 20-22. Therefore, claim 1 is not anticipated by Hofmann, nor are any of the claims depending from claim 1.

Claim 4 recites varying the bias signal with temperature such that it causes the bias current through the grounded base transistor and the current mirror to be proportional to absolute temperature (PTAT). Support for this limitation can be found at page 14, lines 19-21; page 9, lines 20-22; and elsewhere. Hofmann does not disclose the use of a PTAT bias current. The Examiner apparently alleges that this PTAT limitation is disclosed in Fig. 2 of Hofmann, but the description of the circuitry in Fig. 2 of Hofmann at col. 5, lines 31-58 only describes circuitry that is intended to minimize the effect of the bias current. Thus, claim 4 is not anticipated by Hofmann.

Claim 8 recites that the bias signal generator generates a bias signal that varies with temperature such that it causes the bias current through each of the transistors to be proportional to absolute temperature. As discussed above with respect to claim 4, Hofmann does not disclose any method or apparatus for maintaining PTAT bias currents through the transistors. Therefore, claim 8 is not anticipated by Hofmann.

Applicant requests reconsideration in view of the foregoing amendments and remarks. The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears than an interview would be helpful in advancing the case.

Respectfully submitted,

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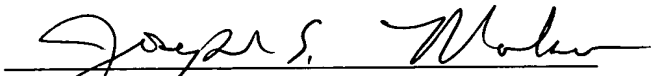

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (Amended) A method for operating a transistor cell comprising an input terminal for receiving an input signal, an output terminal for transmitting an output signal, a grounded base transistor coupled between the input and output terminals, and a current mirror coupled between the input and output terminals, the method comprising:

biasing the transistor cell to establish a bias current in the grounded base transistor and the current mirror when the input signal is zero[.]; and

limiting the input signal to a range in which the output function of the transistor cell approximates a square-law.

2. (Cancelled)

3. (Amended) A method according to claim [2] 1 further including adjusting the bias current, thereby adjusting the input impedance of the cell.

8. (Amended) A squaring cell comprising:

an input terminal;

an output terminal;

a grounded base transistor coupled between the input and output terminals;

a current mirror coupled between the input and output terminals; and

a bias signal generator coupled to the grounded base transistor to establish a bias current through the grounded base transistor and the current mirror[.], wherein the bias signal generator generates a bias signal that varies with temperature such that it causes the bias current through each of the transistors to be proportional to absolute temperature.

13. (Cancelled)

Claim 15 is new.